Ground Support Electronics for Testing the Preflight Performance of the MAXI-GSC

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ABSTRACT

MAXI is an X-ray all-sky monitor which will be mounted on the Japanese Experimental Module (JEM) of the International Space Station (ISS) in 2008. The Gas Slit Camera (GSC) consists of 12 one-dimensional position sensitive proportional counters and the sensitivity will be as high as 1 mCrab for a one-week accumulation in the 2−30 keV band. In order to calibrate the detectors and electronic systems thoroughly before the launch, a fast and versatile Ground Support Electronic (GSE) system is necessary. We have developed a new GSE based on VME I/O boards for a Linux workstation. These boards carry reconfigurable FPGAs of 100,000 gates, together with 16 Mbytes of SDRAM. As a demonstration application of using this GSE, we have tested the positional response of a GSC engineering counter. We present a schematic view of the GSE highlighting the functional design, together with a future vision of the ground testing of the GSC flight counters and digital associated processor.

Keywords: Monitor of All-sky X-ray Image, Ground Support Electronics, reconfigurable FPGA

1. INTRODUCTION

The field programmable gate array (FPGA) was introduced in the mid-1980's as a single purpose technology, a modest device with no function beyond processing digital logic. Today, this adaptable technology has revolutionized the fields of computation and digital logic. While programmable logic devices (PLDs) are built for two-level logic processing, FPGA's are designed for multilevel circuits, with the result that they can handle much more complex circuits on a single chip. With these technologies, however, hardware is indeed "hard", and once an architecture is dedicated to silicon, changes and corrections are difficult to make to the device. Therefore, a system using FPGAs was believed to be less advantageous, especially in proto-typing stage which usually requires redesign and reprogramming for circuit changes.

In the late 1980's and early 1990's, the industry began to develop a new type of FPGA – the static memory (SRAM) based FPGA.[1,4] Since these devices use SRAM cells as the programming technology, the internal architecture as well as interconnections can be reconfigured whenever the system is powered up. Thus, these systems can be thought of containing "soft hardware". Their configurations can be easily changed to upgrade systems or correct system bugs, making them ideal for proto-typing. A user can design precisely the special hardware for a given task without constructing a new hardware for each application. Careful checks and measurements using test circuits can be made easily, instead of running complicated simulations. Considering the development platforms, hardware description language (HDL) and synthesis tools can greatly decrease design time of FPGAs. In most situations, a description based on HDL is easier to understand than the graphical schematic of a complicated gate format.

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In our previous paper in 1998,[5] we reported the application of such new types of flexible device to the ground support electronics (GSE) for testing the Hard X-ray Detector onboard Astro-E satellite. The kernel of this system was a reconfigurable FPGA with 50,000 gates and 1 Mbyte SRAM device, implemented on VME I/O boards. The data acquisition and command operation were controlled by a SUN Sparcstation (CPU-5CE/32). The data obtained were then transfered to another workstation (DEC α PC164: 433 MHz) via an ethernet, since a fast CPU and larger memory are necessary for the detailed analysis and recoding of the data. As a result of recent advances in the field of electronic devices, higher density FPGAs with low power consumption have become available. There has also been dramatic progress in memory devices and computers, such as the advent of synchronous dynamic RAMs (SDRAMs) operating at $\geq$ 100 MHz clock. Moreover, personal computers equipped with fast CPUs and large memories (e.g., 1.3 GHz CPU with 1 Gbyte memory) are available at reasonable prices. Taking account of these technical innovations, the GSE could be made more compact and convenient for testing the future astrophysical missions, such as MAXI[6] and Astro-E II.[3]

The first astronomical payload to be placed on the International Space Station (ISS)'s Japanese Experimental Module (JEM) is the Monitor of All-sky X-ray Image module (MAXI). MAXI will be launched by the H-II A rocket in 2008 and will scan the whole sky every 90 minutes through 1.5 degree-wide slits, using GAS Slit Camera (GSC) sensitive in the 2$-$30 keV band[7, 12] and with Solid-state Slit Camera (SSC) covering the 0.5$-$10 keV band.[9, 10, 14] The detector sensitivity will be at the level of 7 mCrab (5 σ level) in one scan and 1 mCrab in a one-week accumulation, exhibiting the highest sensitivity ever observed in an all-sky monitor. Full details of a MAXI mission are given in Isobe et al (2003) in this volume and also in literature.[6, 8, 15] The data from the sensor sections (GSC, SSC) are processed by the analog electronics (MDP) and the digital processor (DP), specifically designed for the modular configuration of the MAXI (§2.1). The GSC/SSC sensors, MDP and DP are being constructed by several different companies and manufacturers.

Obviously, functionalities provided by the DP are necessary to test the flight sensors and electronics. However, the DP will only be available at the final stage of system integration. In addition, we need sensors and MDP to test the DP, but these will not be available until just before launch. To simulate the various functionalities of sensors, MDP and DP, and to calibrate the detectors and electronic systems thoroughly before the launch, we have developed a new GSE based on VME I/O boards for a Linux workstation. The kernel of this system is a reconfigurable SRAM based FPGA with 100,000 gates, tightly coupled to 16 Mbytes SDRAM (133 MHz clock). We give an overview of the data flow of the MAXI in §2, and configuration of the GSE in §3, presenting the schematic view of the functionality of our design. In §4, the performance tests of the GSC sensor using the newly developed VME I/O board are presented. We present our conclusion in §5.

2. DETECTOR SYSTEM OF THE MAXI

2.1. Data Flow

As we have briefly reviewed above, the detector system of MAXI consists of a sensor section (GSC,SSC), the mission data processor (MDP), and the digital processor (DP). Figure 1 shows the pictures of individual components of the MAXI detector system : GSC (*right*), MDP(*middle*), and DP(*right*). The GSC consists of 12 cameras with a total geometrical area of 5,350 cm^2, whereas the SSC is comprised of CCD arrays with a total area of 200 cm^2 (25$\times$25 mm for 1 chip). There is also a further support sensor, namely a Radiation Belt Monitor (RBM), to monitor the charged particle flux and interrupt the high voltage of GSC for protection. The MDP receives the photon event data from the GSC and SSC, and digitizes the data. The DP reformats and reprocesses the data from the MDP. It reacts to requests for services and provides the primary interface with the JEM/ISS for commands and telemetry. There are two interfaces between MAXI and the JEM Exposed Facility (JEM-EF): a medium-speed interface (10Base-T ethernet) and a low-speed interface (MIL1553B). The data via the former interface is transmitted to the ground station using USA data relay satellites TDRSS, whereas the latter uses Japanese data relay satellite DRTS. All the observational data are finally sent to the Tsukuba center in JAPAN. The MAXI data flow is shown in figure 2.

Looking into more detail, MDP consists of GSCE-A, GSCE-B, and SSCE. MDP supplies power to the sensors, format the observational data, and monitors various conditions of GSC and SSC units. The 3 cameras out of 6 in the zenithal view (GSC-H) and 3 out of 6 in the horizontal view (GSC-Z) are connected to GSC Electronics-A

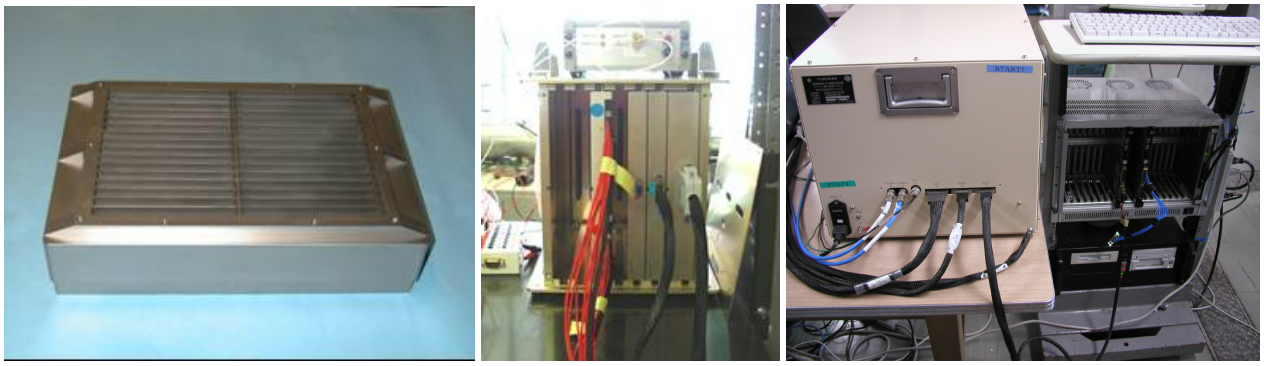

Figure 1. Detector unit of the MAXI. *left*: GSC flight counter (one unit), *middle*: Mission Data Processor (MDP), and *right*: Digital Processor (DP R2).

(GSCE-A), and the rest in each views are connected GSC Electronics-B (GSCE-B) in order to average the load of data handling. Two SSC cameras, horizontal and zenith, contains 16 CCD chips each, and are fed into the SSCE. GSCE carries analog shaping amplifier, clock counter, and 14 bit analog to digital converter (ADC). SSCE carries the driver board and readout board for processing the CCD video signal. The CCD signal is converted by 12bit ADC and transfered to the DP.

The DP is constructed on the VME bus. The size of the DP box is 52×32×31.5 cm, and the weight is 44 kg and power consumption is 79 W in total. The DP carries four CPU modules, one memory module (EEROM 6 Mbyte), interfaces to the GSCE and SSCE, and interfaces to the payload bus. Two identical CPU modules are used for master and sub-master, which handle communication and GSC data handling. There are other two identical CPU slave modules for SSC data processing. Even when one CPU modules fails in each set, another CPU module can continue its function in a reduced mode. The common memory module is used to store the information of the observation parameters and default configuration of CPUs (i.e., which modules work as the master or slave). There are also interfaces for the support sensors; VSC I/F and GPS I/F.

2.2. Data Types

The data from the MAXI sensors (GSC and SSC) are classified into two groups: observational data and monitor data. The observational data of the GSC includes pulse height information (28 bit; 14 bit each from the right and left sides of an anode), arrival time of each photon event (16 bit), hit pattern on the anode wires (8bit), and data ID bits (12 bit). The GSC monitor data consists of a scaler count from each of anode wires, RBM data, and GPS stamp data. The temperature of the GSC sensors and the status of high voltage are monitored in a housekeeping (HK) data stream. Event data provides random triggers up to the maximum count-rate of 1969 cts/sec, determined by a serial transfer limit (see below). Scaler data, GPS stamp data, and RBM data are collected every 1 sec, whereas HK data are sent to the DP every 10 sec. SSC observational data consists of pulse height information from 16 CCD chips (12 bit×1024 pixels: 64 lines), over clock data (12 bit×16), and ID bits (24 bit). SSC-HK data includes operation mode information, temperature of the CCD chips, monitoring of the CCD drive voltage, etc.

2.3. Interface between the MDP and DP

The MDP and DP are connected via bi-directional serial lines. Figure 3 shows an interface between the MDP(GSCE) and the DP. The MDP sends GSC observational data to the DP, while the commands for the operation of sensors and MDP are sent from DP by serial lines in the reverse direction. The clock frequency is 128k bps. For the GSC, the command length is 4 byte (250 μs/command) and the data length is 8 byte (500 μs/event). The transfer rate and length of the SSC command is exactly same as those of the GSC (128k bps and 4 byte length). Meanwhile, the observational data of SSC are sent to DP continuously by using 2M bps clock signals. Moreover, the data length is variable. The SSC HK data are sent to the DP using different clock signals at 125 bps.

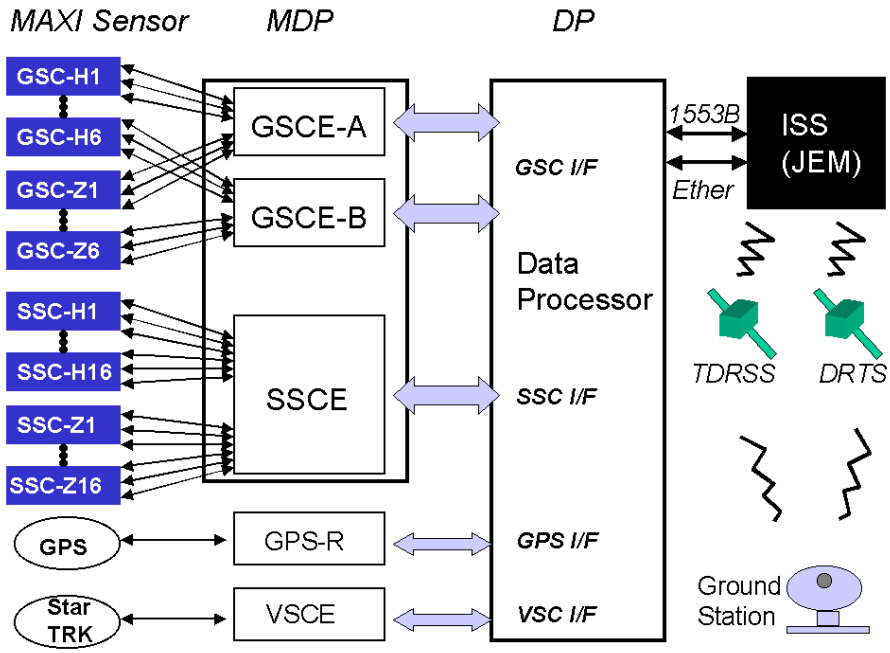

Figure 2. The block diagram of the MAXI data flow. The X-ray events are detected by the MAXI sensor, digitized and formatted in the MDP, and sent to the ground station through the DP. Full details are given in the text.

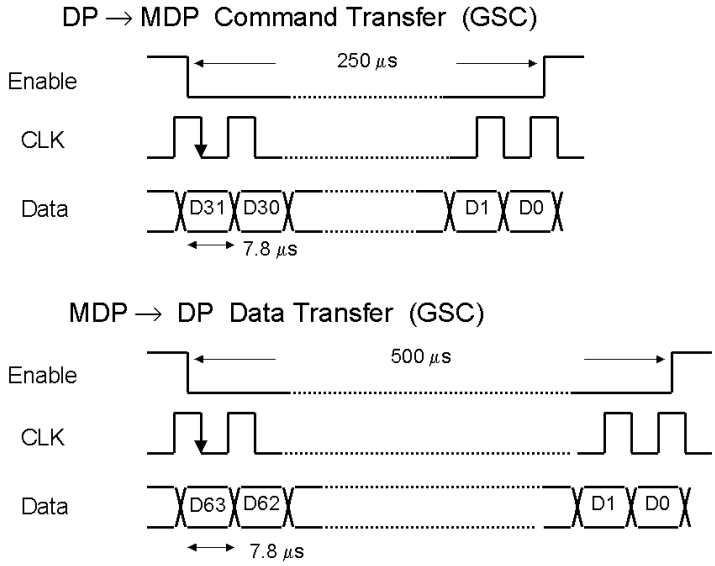

Figure 3. Serial interfaces between the MDP and the DP for GSC command and data transfer.

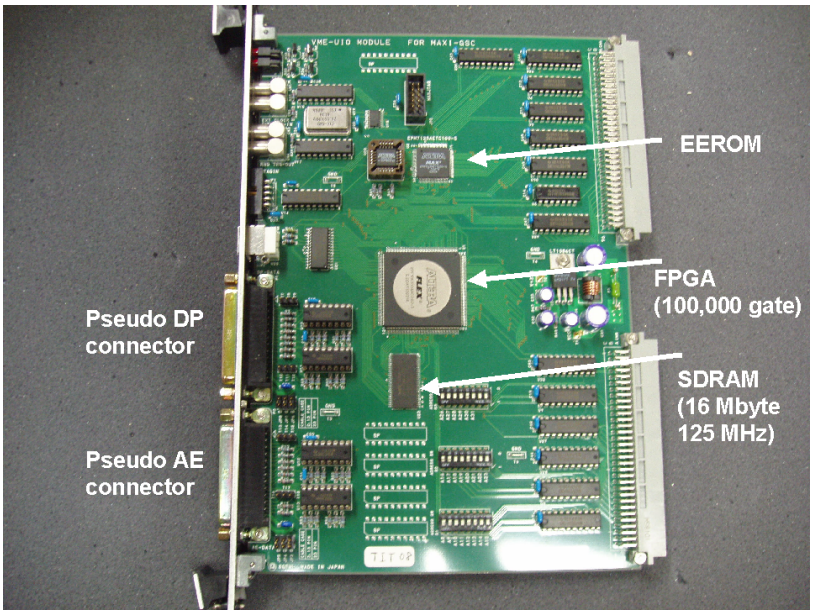

Figure 4. A view of the VME I/O board developed in this paper. This board carries a reconfigurable FPGA of 100,000 gates, a 16 Mbyte SDRAM, and interfaces between the VME bus.

3. DEVELOPMENT OF THE GROUND SUPPORT ELECTRONICS

In order to provide convenient environments for testing flight systems of the MAXI, we have developed a versatile GSE using a reconfigurable FPGA, implemented on VME I/O board. The outstanding property of this GSE is that it can realize almost all the functionalities of the sensors, the MDP and the DP, only by selecting the configuration program downloaded to the FPGA device. A Linux machine (1GHz clock, 512 Mbyte memory) reads data stored in each of the VME I/O boards through the SBS Bit 3 616/617 (VME bus−PCI bus bridge). Since the purpose of this paper is to build up ground support electronics for MAXI-GSC, we will focus on the handling of GSC data in the following discussion. A detailed description of the SSC is given in literature,[9,10,14] and Miyata et al. (2003) in this volume.

3.1. Design of the VME I/O board

We have designed a new VME I/O board (6U double-height) incorporating a reconfigurable FPGAs (FLEX 10K100A) and with 16 Mbyte SDRAM (μPD45128441), tightly coupled to each FPGA device. Figure 4 shows a picture of the VME I/O board developed in this paper. For the interface between the FPGA and VME-bus, we used an EEROM (MAX7000). Hardware connections for each device are shown schematically in Figure 5 (*left*). The functional design of each device, as well as data flow are given in Figure 5 (*right*). Note that this board carries two D-sub connectors for possible use as a pseudo-DP or pseudo-MDP (see § 3.2 and § 3.3).

The FLEX 10K family, being Altera's recent family of CMOS devices, provides the flexibility of traditional programmable logic together with the efficiency and density of embedded gate arrays.[13] FLEX 10K100A is an SRAM based FPGA with 100,000 gates, and operates at 3.3 V supply voltage. It is an average of 20−30 % faster than usual FLEX 10K device, which operates at 5.0 V. More than 400 I/O pins are available to the user. Each FLEX 10K100KA device contains 4,992 logic elements, 624 logic array blocks and 12 embedded array blocks. The configuration data of the newly designed circuit has a tabular ASCII format and is loaded from a Linux workstation via a PCI-VME device driver. One can also use the serial JTAG port, included on VME I/O board for the configuration. Throughout the development, we used the MAX+PLUS II compiler system, also provided by the Altera corporation. We designed all the circuits using Text Design Files (TDF) written in Altera hardware description language (AHDL).

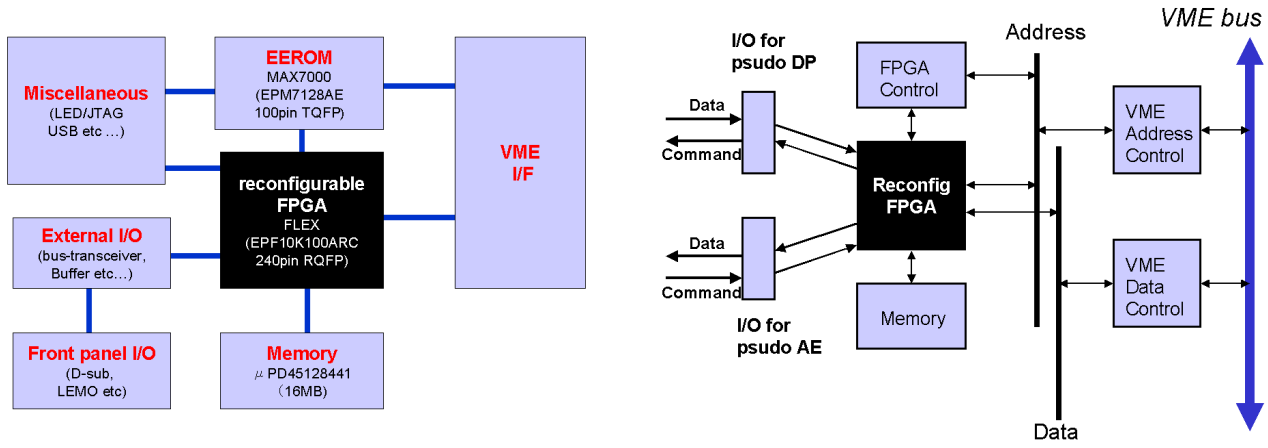

Figure 5. *left*: Hardware connection of each device on the VME I/O board. *right*: The functional design of the VME I/O board.

3.2. Design of GSE as a pseudo-DP

The prime motivation for developing the GSE is to test the performance of the GSC flight sensors and read-out electronics. At present, 5 out of 12 flight model counters (FM) have been built by the Metorex Company, Finland (FM-005,006,007,008). Also, three engineering model counters (EM: almost equivalent to the FM) have been tested to study the energy response (resolution and linearity) and position resolution of each counter. These GSC counters are connected to the MDP (GSCE) proto-model, constructed by Meisei Electric K.K. In order to test the counter response through analog electronics, we first realized the major functionalities of DP with our GSE. A schematic design for the performance test is shown in Figure 6. Two VME I/O boards can handle the data from 12 GSC counters: one is connected to GSCE-A and the other is connected to the GSCE-B.

When a send request is made from a computer, for example to power-on the high voltage and to increase the amplifier gain, these command data are first sent to the register on the FLEX device through VME bus. The contents of the register will be checked immediately (within 40 nsec) and arranged into a serial format, to be transmitted to the MDP via the RS422 serial port (D-sub 25 pin). Meanwhile, the GSC event data are sent from the MDP, and are injected into the FLEX device via the input port. These data are arranged into a parallel format to be sent to the memory device on the board. Data stored in the memory can be read via the VME bus, by pointing to the address where the memory is mapped. Only one Linux machine is needed for recording and analyzing the GSC data. Furthermore, event rate and pulse height histograms can be checked in real time, providing real-time monitoring of GSC data.

A double buffer configuration is one of the more effective and easiest ways to design a fast data acquisition system. A 16 Mbyte SDRAM device on each GSE board is divided into two identical buffers A and B by designating the pointer (Figure 7). The data accumulated in one side of the buffer can be read without interfering with the write cycle processing on the other side. By changing the readout buffer cyclically, a ring buffer of effectively infinite memory size can be constructed. Each 8 Mbyte buffer consists of a pair of 4 Mbyte memory blocks: one is used to store the data size received from the MDP and packet pointer for each event, and the other is shared as a cache of raw GSC data (8 byte/event). In our design, a pointer to the n-th data packet is recorded at the $(2n+1)$-th word at the top of the memory, with the data size being stored at $2n$-th word. By referring to the pointer and a size of the data for the n-th packet, one can easily access the raw data stored in another cache of the memory block. In the erroneous case that the data are not read out before the memory overflows, the incrementing of the pointer will be stopped automatically, thus avoiding the overwriting of stored data.

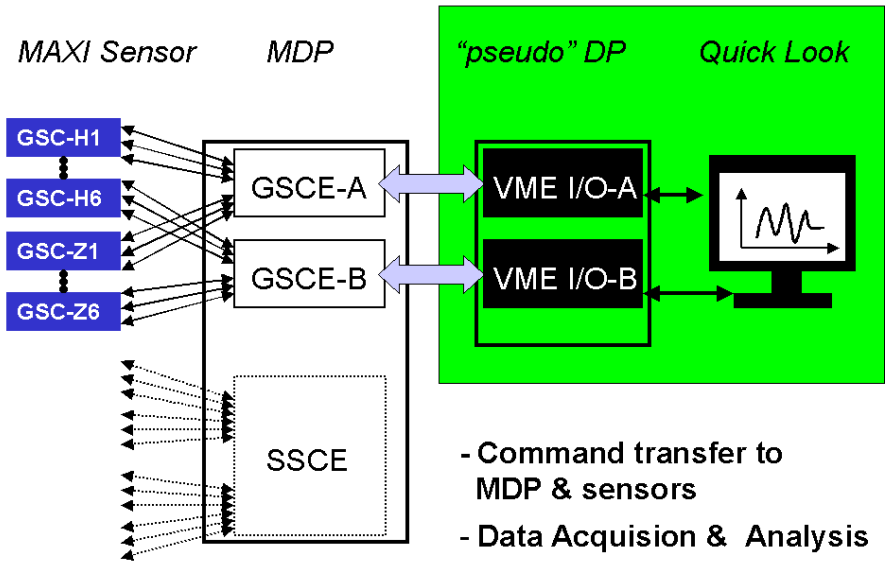

Figure 6. A schematic design of the performance test of GSC counters and MDP. The VME I/O boards work as a pseudo-DP, and are controlled by a Linux workstation.

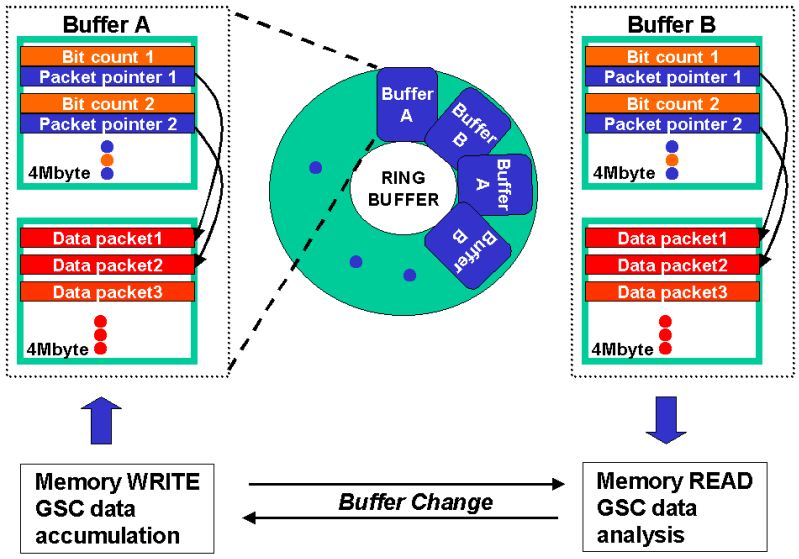

Figure 7. *left*: A memory configuration of the GSE as a pseudo-DP. *right*: A ring buffer of virtually infinite memory size is constructed by changing the double buffer at a constant interval.

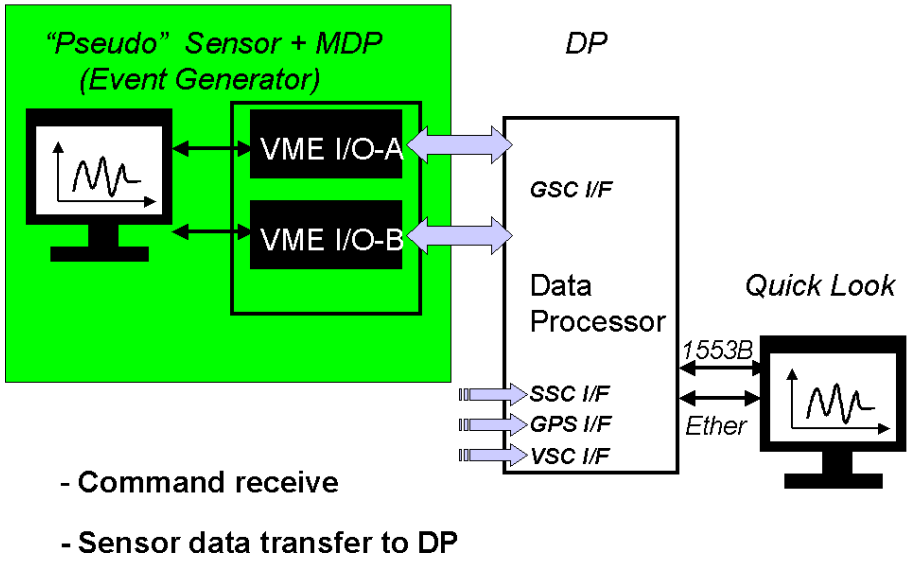

Figure 8. A schematic design of the performance test of the DP. In this case, the VME I/O boards can work as a pseudo-MDP(or sensors), which react to commands and generate pseudo signals at arbitrary output rates.

3.3. Design of GSE as a pseudo-MDP and Sensors

In the development phase of the MAXI systems, further requests have been made to test the detailed performance of the DP proto-type model. The performance of the first proto-type model (DP-R1) has been reported in Mihara et al (2001), but it differs from the flight DP in many aspects. The second proto-type (DP-R2) was constructed by NEC-TOSHIBA Space System Ltd and released very recently (April 2003). Basic functions of DP-R2 are exactly same as the flight model: it carries four CPU modules, interfaces to all sensors, and is equipped with 1553/ethernet ports. In order to test the DP (R2) without connecting actual MAXI sensors (GSC and SSC), we constructed the "pseudo-MDP" , functioning as a realistic simulator of the GSC and GSCE. A schematic design of the performance test of DP (R2) is shown in Figure 8. Two VME I/O boards are connected to the interface ports of DP(R2) via serial RS 422 lines. Note that the hardware design of VME I/O board is exactly same as those used in § 3.2. The only difference is in the configuration program downloaded to the FPGA device on the VME I/O board.

The DP sends operational commands to the MDP (i.e., GSE) at requested times. It also sends "GPS request" commands at constant a time interval (every 1 sec) to stamp the time on each GSC event data. Once the command is received by the GSE, an arrival flag is generated and the command is checked with a list on a Linux machine. If the command is not on the list, the GSE will take no action, but otherwise it reacts to the commands for output corresponding GSC data. For example, if the "GPS request" is received, the GSE generates GPS data and replies to the DP immediately. If the command is "GSC power on", the pseudo-GSC data are read out from the memory device by pointing to the address of the data stored region. These pseudo-events are finally transmitted to the DP via the RS422 serial port (D-sub 25 pin).

In order to output various GSC data patterns at arbitrary event rates, we grouped the memory into data packets of 3 word lengths as shown in Figure 9. The first 1 word (*timing*) defines the output rate of the GSC data, and succeeding 2 words are raw data. The GSC data will be output after waiting for $(timing/f)$ [sec], where f is the clock frequency (24 MHz for our case). By changing the *timing* from 0 to 2^{31}, data will be output with an arbitrary delay of 0 nsec – 89.5 sec. Therefore, we can easily adjust event rates from 0.01 cts/s to

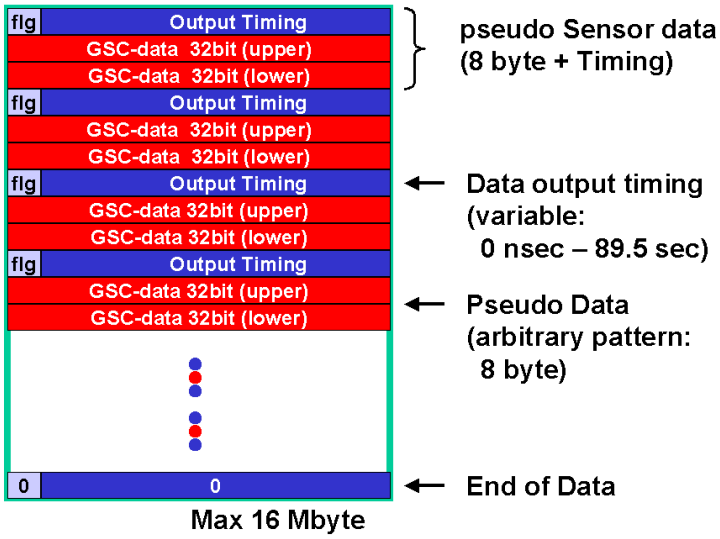

Figure 9. A memory configuration of the GSE as a psudo-AE. Output event rates can be controlled by changing the "Output Timing" data from 0 to 2^{31}.

1969 cts/s, and switch the periodic/random output. For example, if we set the GSC event rate to 10 cts/s/GSC expected in orbit, we can generate pseudo events of different patterns for more than 6 hours without reloading the data to the memory. One can revise data stored in the memory device at any time, without interrupting the MDP-DP communications. Our GSE provides a convenient and flexible environment for testing the DP in various situations expected in orbit.

4. PERFORMANCE TEST OF THE MAXI-GSC (ENGINEERING MODEL + MDP)

Finally, we present an example of a performance test of the MAXI-GSC, based on the engineering model sensor (EM02) and MDP (GSCE). This engineering counter was built by Metorex Company, Finland. It is called "engineering", but actually the equivalent to the 2nd counter of the flight model, in the sense that it is of sufficiently high quality to be used in space. The setup of the experiment is same as in Figure 6, except that only a single GSC counter is connected. In order to investigate the positional dependence of GSC, a pencil X-ray beam (Cu K_α: 8.0 keV) was injected to the counter. One-to-one correspondence between the pulse-height data and sensor position was obtained automatically by recording the position of stage controller at the beginning of data acquisition.

A GSC counter has the window size of 27.2×19.0 cm, which is about A4-paper size. The opening area is 445.9 cm^2. The gas is the mixture of Xe and CO_2 with total pressure of 1.4 atm at 0°C. The carbon fibers with a diameter of 10 μm are used as anodes. The anode resistance is about 33 kΩ, and the wire length is 333 mm. The position of the injected X-ray photons is obtained using the charge division method. The preamplifiers (A225 hybrid IC) are connected to both ends of the anode, and both pulse heights from the left PH_L and from the right PH_R are recorded at the same time. The "position measure" PM is defined as $PM = (PH_R - PH_L)/(PH_R + PH_L)$ (Figure 10 *left*). The incident X-ray positions, namely the direction of celestial X-ray sources, are determined by PM using the calibration curve.

To obtain good position resolution with the GSC, a large pulse height is preferred since the noise is dominated by Johnson noise of the resistive anode. In this case, the positional resolution is determined by pulse height and radius of the anode wire; $\Delta X/X \propto PH^{-1}r^{0.5}$. Thinner wires with higher resistance would improve the positional resolution, but 10μm is almost at the limit of practical handling. While the higher bias voltage (i.e.,

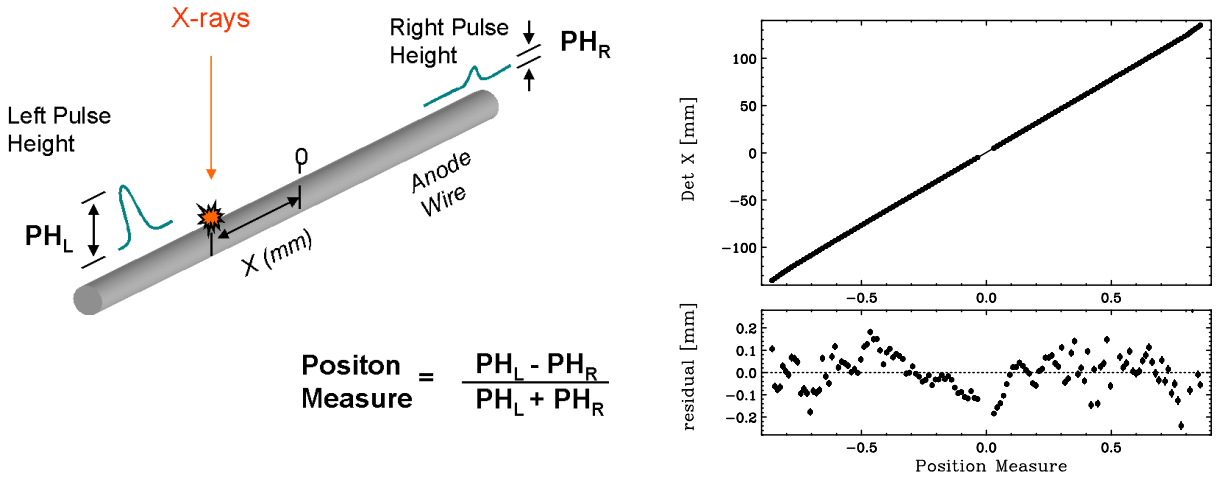

Figure 10. *left*: The concept of charge division method. The incident X-ray positions are determined by the position measure (PM) using the calibration curve. *right*: The relation between PM and the position of the incident X-ray photon on one anode wire (C3 of EM02 counter; at 8.0keV). Lower panel shows the residual to the best fit curve.

higher pulse height) improves the positional resolution, energy resolution becomes worse due to enhancement of the gain difference between cells of the GSC. Moreover, we will encounter the "hard tail" problem as discussed in Mihara et al. (2002). Therefore, we intend to operate the GSC counter (EM02) at a bias voltage of 1650 V, in order to avoid significant degradation of energy resolution.

The relation between the position measure (PM) and the position of the X-ray injection on one anode (C3) is shown in Figure 10 (*right* upper). The PM was calculated from the left to right of the anode wire: $X = -135 \sim 135$ mm in 2 mm steps. The relation is roughly approximated by a linear function, but to reduce the residuals further, the PM is fitted by a function of the form $X = a_0 + a_1 PM - a_2 /(PM - a_4) - a_3/(PM - a_5)$, where $a_0 \sim a_5$ are constants. This empirical equation represents the PM curve well, within errors of $\pm$ 0.2 mm. Residuals to this model is shown in Figure 10 (*right* lower). It is known that such a residuals are appropriate to this anode. When producing the response matrix of the GSC, we have to take these deviations into account in order to obtain more precise positioning for all anodes in all GSC counters.

The positional dependence of the pulse height along the anode wire (X direction), is shown in Figure 11, together with the position resolutions. The pulse height tends to be higher at the end of the anode wire, but almost flat. However, the positional resolution changes from 1.4 mm near the center, gradually degrade to 2.3 mm at the edge of the anode. Obviously, the positional resolution should be flat and independent of the X-ray injected position. We found that such a trend could be eliminated if the same GSC counters are tested without the MDP (i.e., using discrete shaping amplifiers and ADC in the laboratory system). We are investigating the noise or time-constant of shaping amplifiers in the MDP, and this will be fixed in the second test model of the MDP.

Further tests of MAXI systems, including sensors and DP(R2), are now in progress. Figure 12 shows the overall schedule of the MAXI project. We will test the response of flight GSC counters and flight DP model by using the GSE reviewed in this paper.

5. CONCLUSION

We have developed a fast and versatile GSE on VME I/O board for the ground testing of the MAXI-GSC. This board carries a reconfigurable FPGA with 100,000 gates, together with a 16 Mbyte SDRAM device tightly coupled to each FPGA device. Development and extension of the system was greatly simplified due to the

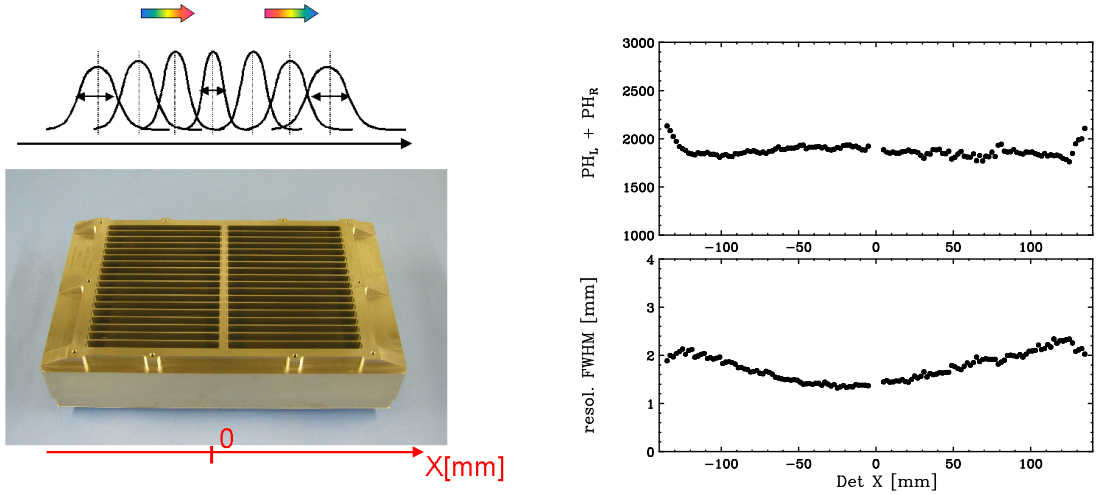

Figure 11. The positional dependence of the pulse height (*upper right*) and positional resolutions (*bottom right*) measured for GSC EM02 counter (*left*) at 8.0 keV X-rays.

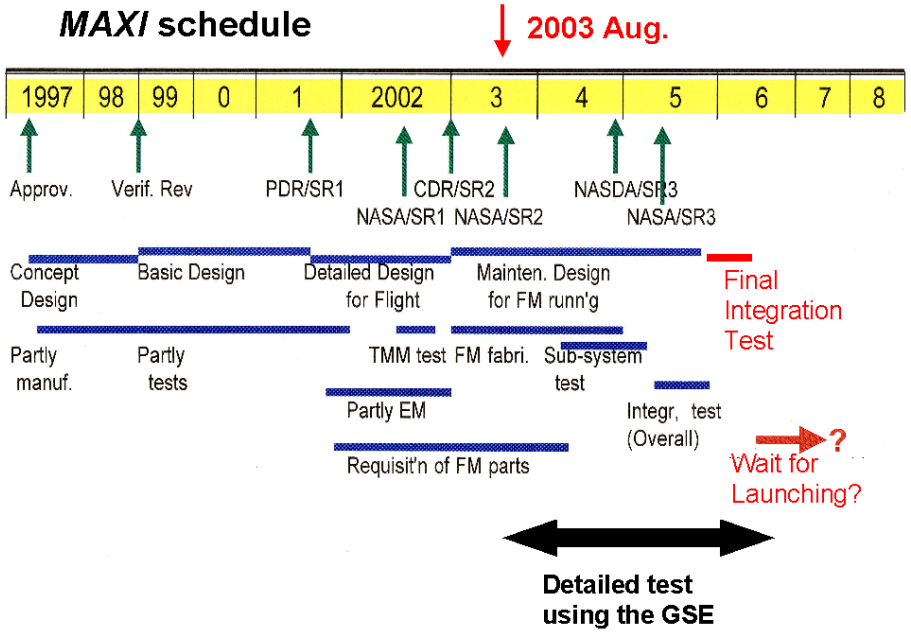

Figure 12. The overall schedule of the MAXI project.

reconfigurability of the FPGA. Most notably, we can realize both the functionalities of sensor+MDP and the DP by merely changing the configuration program downloaded to the FPGA device. Such a FPGA-based flexible system, can be a viable platform for future applications. As an initial result of the ground testing of the MAXI-GSC, we have demonstrated the performance of a single GSC counter (EM02) connected with the MDP. Verification and calibration of the MAXI is now in progress, directing all efforts to the launch in 2008.

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